

Quiz 3

(November 6th @ 5:30 pm)

PROBLEM 1 (30 PTS)

- Complete the timing diagram of the circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity circ is
  port ( rstn, a,b, x, clk: in std_logic;
        q: out std_logic);
end circ;
```

```
architecture xst of circ is
  signal qt: std_logic;
```

```
begin
```

```
  process (rstn, clk, a, b, x)
```

```
  begin
```

```
    if rstn = '0' then
```

```
      qt <= '0';
```

```
    elsif (clk'event and clk = '1') then
```

```
      if x = '1' then
```

```
        qt <= a xnor b;
```

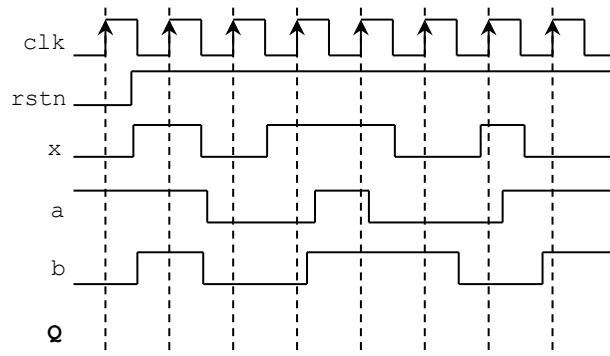
```
      end if;
```

```
    end if;
```

```
  end process;
```

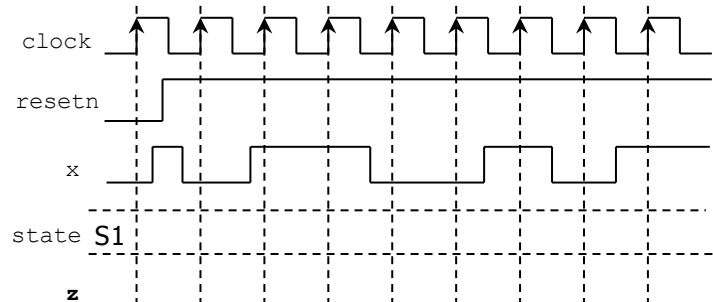
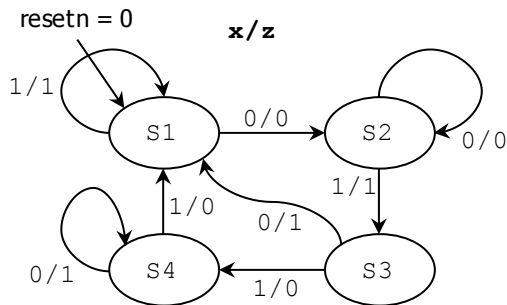
```
  q <= qt;
```

```
end xst;
```



PROBLEM 2 (30 PTS)

- Complete the timing diagram of the following state machine:



PROBLEM 3 (40 PTS)

- Complete the timing diagram of the following circuit:

